User Guide

CC2-TANGO • *CompactPCI* ® Low Power CPU

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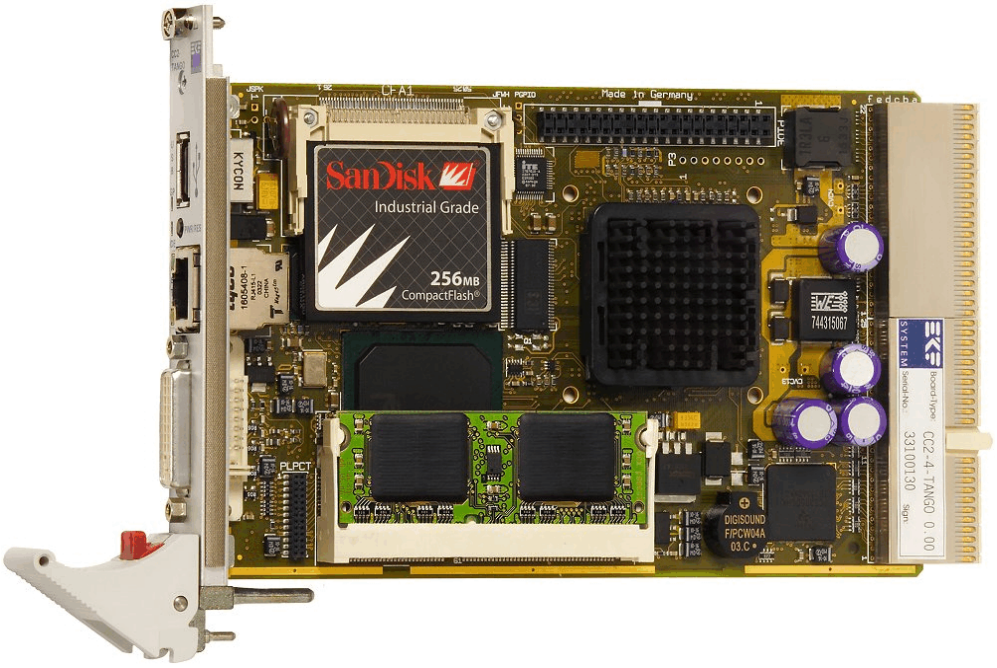

Contents

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About this Manual

This manual describes the technical aspects of the CC2-TANGO, required for installation and system integration. It is intended for the experienced user only.

Edition History

Document	Ed.	Contents/*Changes*	Author	Date
Text # 3082 cc2_uge.wpd	1	User Manual CC2-TANGO, English, initial edition	jj	5 June 2003
	2	Added information on CCY-RIO rear I/O transition module	jj	21 July 2003
	3	Added Component Assembly Drawing	jj	20 August 2003
	4	Added photos	jj	16 December 2003
	5	Added MTBF Added information on CC0-CHILLOUT Expansion Module	jj	22 April 2004
	6	Corrected table & illustration Ethernet connector	jj	16 June 2004
	7	Modified table Feature Summary: - Added PCMark2002 Scores - Added Shock/Vibration/Altitude Modified block diagram CC2-TANGO Added chapter on CCZ-RIO	jj	14 October 2004
	8	Added description of jumper JRTC	jj	8 June 2005
	9	Added maximum power consumption CC2-1 CC2-2 to table 'Feature Summary'	jj	13 June 2005
	10	Table 'Feature Summary', changed maximum IDE transfer mode to Ultra ATA/100	jj	9 October 2006

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Related Documents

For information about the CC6-ACID refer to the CC6 Technical Information Manual, available at http://www.ekf.de/c/ccpu/cc6/cc6.html.

For information about the CC0-CHILLOUT refer to the CC0 Technical Information Manual, available at http://www/c/ccpu/cc6/cc6.html.

For information regarding the CCY-RIO rear I/O transition module please read the CCY Technical Information Manual, available at http://www.ekf.de/c/ccpu/cc2/cc2_e.html.

For a description of the CC2-TANGO BIOS see document 'CC2-TANGO BIOS Quick Reference', available by download at http://www.ekf.de/c/ccpu/cc2/cc2_e.html (document currently not yet available).

For ordering information refer to document CC2-TANGO Product Information, available at http://www.ekf.de/c/ccpu/cc2/cc2_pie.pdf

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

Intel, Pentium, Celeron, Tualatin, Coppermine: ® Intel
CompactPCI: ® PICMG
Windows 98, Windows NT, Windows 2000, Windows XP: ® Microsoft

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

CC2-TANGO Features

Feature Summary

Feature Summary CC2-TANGO	
Form Factor	Single size *CompactPCI* style Eurocard (160x100mm^2), front panel width 4HP (20.3mm)
Processor	Designed for Intel® ULV Celeron® and LV Pentium® III Micro FC-BGA processors (Tualatin 0.13 generation), maximum junction temperature 100°C • CC2-1: 400MHz ULV Celeron, 0.95V, 100MHz FSB, 256KB L2 cache, 3.4W typical 4.2W max. • CC2-2: 650MHz ULV Celeron, 1.10V, 100MHz FSB, 256KB L2 cache, 7.0W typical 8.3W max. • CC2-3: 800MHz LV Pentium 3, 1.15V, 133MHz FSB, 512KB L2 cache, 11.2W max. • CC2-4: 933MHz LV Pentium 3, 1.15V, 133MHz FSB, 512KB L2 cache, 12.2W max.
Chipset	Intel® i815 chipset consisting of: • 82815 Graphics/Memory Controller Hub (GMCH) • 82801 I/O Controller Hub (ICH2) • 82802 Firmware Hub (FWH)
Memory	• 144-pin SO-DIMM socket • Support for up to 512MB, PC133, non ECC, unbuffered SDRAM • Support for serial presence detect (SPD) and non-SPD SO-DIMMs
Video I/O	Analog monitor and digital flat-panel display support by DVI-I connector (front panel), up to 1280x1024 pixel 16M colors 85Hz refresh rate, incorporates PanelLink Digital technology (Silicon Image). Option: D-SUB (female HD15) connector available, replaces DVI-I connector
USB I/O	Ports over-current protected, data transfer rate of up to 12Mbps, conforming to USB1.1 • USB port 1: Type A connector (front panel) • USB port 2: J2/P2 Rear I/O option
Ethernet I/O	10/100Mbps Fast Ethernet controller, 82551ER chip, RJ45
Legacy I/O	• LPC Super-I/O interface connector, CC6-ACID and CC0-CHILLOUT companion boards available • J2/P2 Rear I/O option: Keyboard, Mouse, COM1 (TTL only)
IDE/ATA	• Ultra ATA/100 40-pin connector (primary IDE) • CompactFlash socket for CFA ATA cards (secondary IDE) • J2/P2 Rear I/O option: Primary IDE
CompactPCI	32-bit, 33.3MHz, PCI bridge chip Texas Instruments PCI2050, 133MBps CPCI master

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J2/P2 Rear I/O Option	• Primary IDE • USB Port 2 • Keyboard, Mouse • COM1 (TTL Level) • Rear I/O transition module CCY-RIO available			
PXI Support	TRIG0, TRIG1, TRIG6, TRIG7 (can be alternatively used as GPIO)			
BIOS	Phoenix BIOS, single or dual FWH (8/16Mbit Flash Memory)			
Power Requirements	• CC2-1-TANGO: +5V±0.25V 1.3A max.+3.3V±0.1V 1.1A max. • CC2-2-TANGO: +5V±0.25V 1.9A max.+3.3V±0.1V 1.3A max.			
Thermal Conditions	Processor heatsink, typical thermal resistance 13.8K/W (natural convection), 4.6K/W (forced airflow @ 200LFM). Custom specific heatsink solutions on request. • CC2-1: 0-40°C (natural convection cooling), 0-70°C * (200LFM forced airflow) • CC2-2: 0-60°C (200LFM forced airflow), 0-70°C * (400LFM) • CC2-3: 0-45°C (200LFM forced airflow), 0-65°C (400LFM), 0-70°C * (600LFM) • CC2-4 0-40°C (200LFM forced airflow), 0-65°C (400LFM), 0-70°C * (600LFM) * Limited to 70°C due to other components than the processor Storage temperature -40°C to +85°C Humidity 5-90% non condensing			
MTBF	0.113 * 10^6h			
Altitude	-300m to +3000m			
Shock	15g 0.33ms, 6g 6ms			
Vibration	1g 5-2000Hz			
Typical Calculating Performance	PCMark2002 under Windows 2000, CPU/MEM Score			
	1274/886 @400MHz	1990/933 @650MHz	tbd @800MHz	2854/1467 @933MHz

Subject to technical changes

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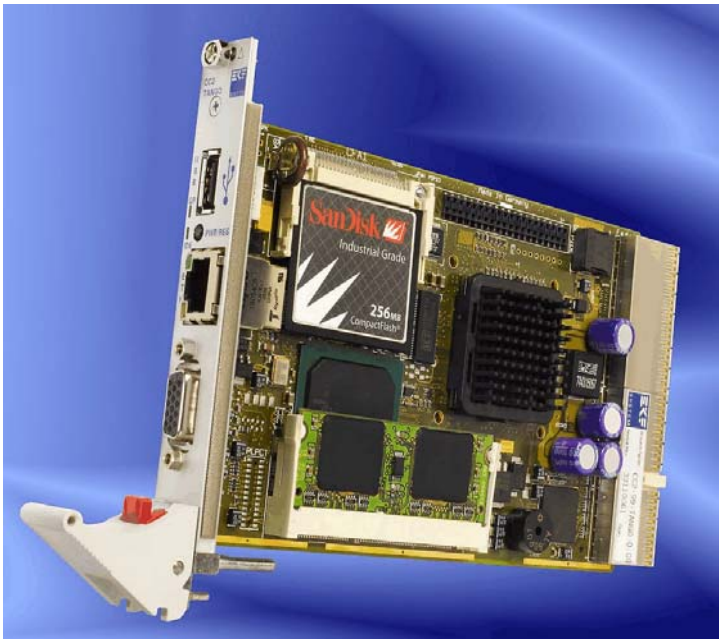
CC2-TANGO (DVI-I)



CC2-TANGO (VGA)

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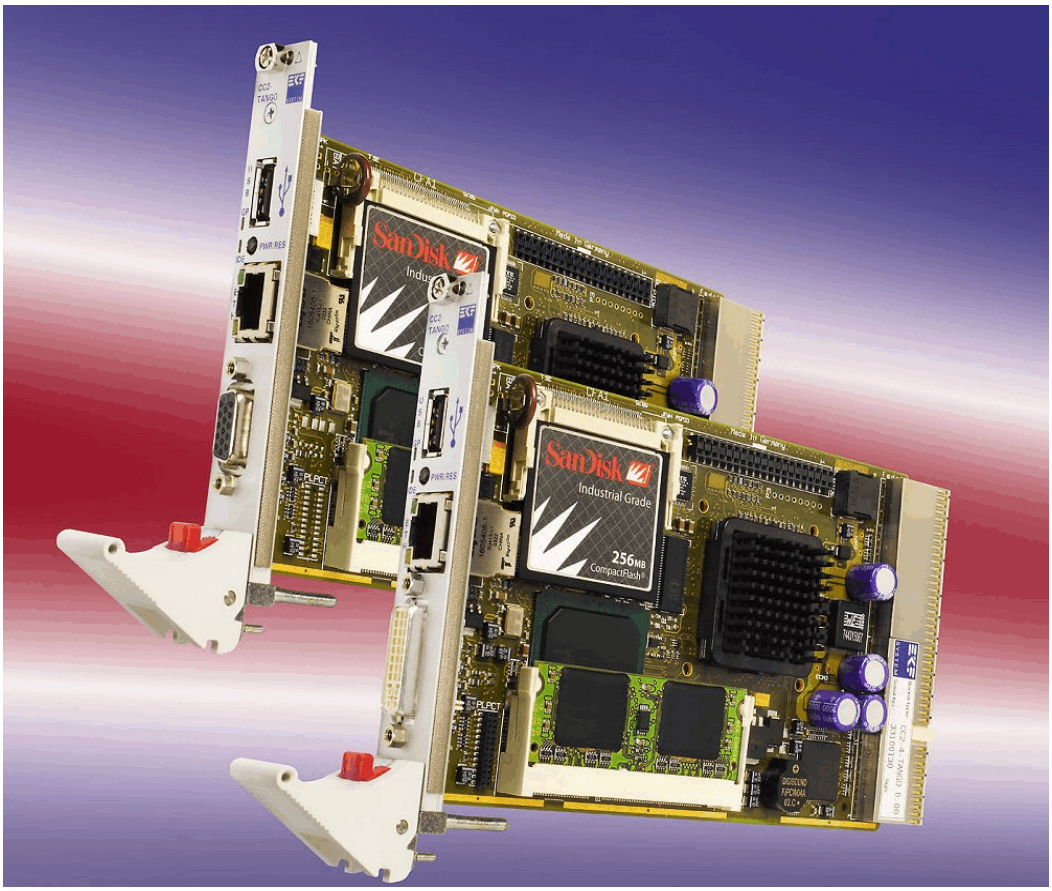
Short Description CC2-TANGO

*Alternatively equipped with the Intel® series of ULV Celeron® or LV Pentium® III processors, the CC2-TANGO is a versatile 4HP/3U (single size Eurocard) **CompactPCI**® CPU board, designed especially for systems which require low power consumption.*

Available either with the 800/933MHz Low Voltage Pentium III or the 400/650MHz Ultra Low Voltage Celeron processor and up to 512MB RAM, the CC2-TANGO covers a wide range of applications, including PXI systems.

The DVI-I video interface allows for attachment of both, advanced (digital) and legacy (analog) flat panel displays and CRT monitors (D-SUB connector optionally). The CC2-TANGO is provided with a Gigabit or 100Mbps Ethernet controller. The on-board CompactFlash socket allows for utilization of an ATA Flash card or IBM Microdrive®. A local expansion interface connector may be used to directly attach a companion I/O board, which can carry also a hard disk drive. As an option, rear I/O across the J2/P2 connector is available.



CC2-TANGO with DVI-I and VGA Video Connector

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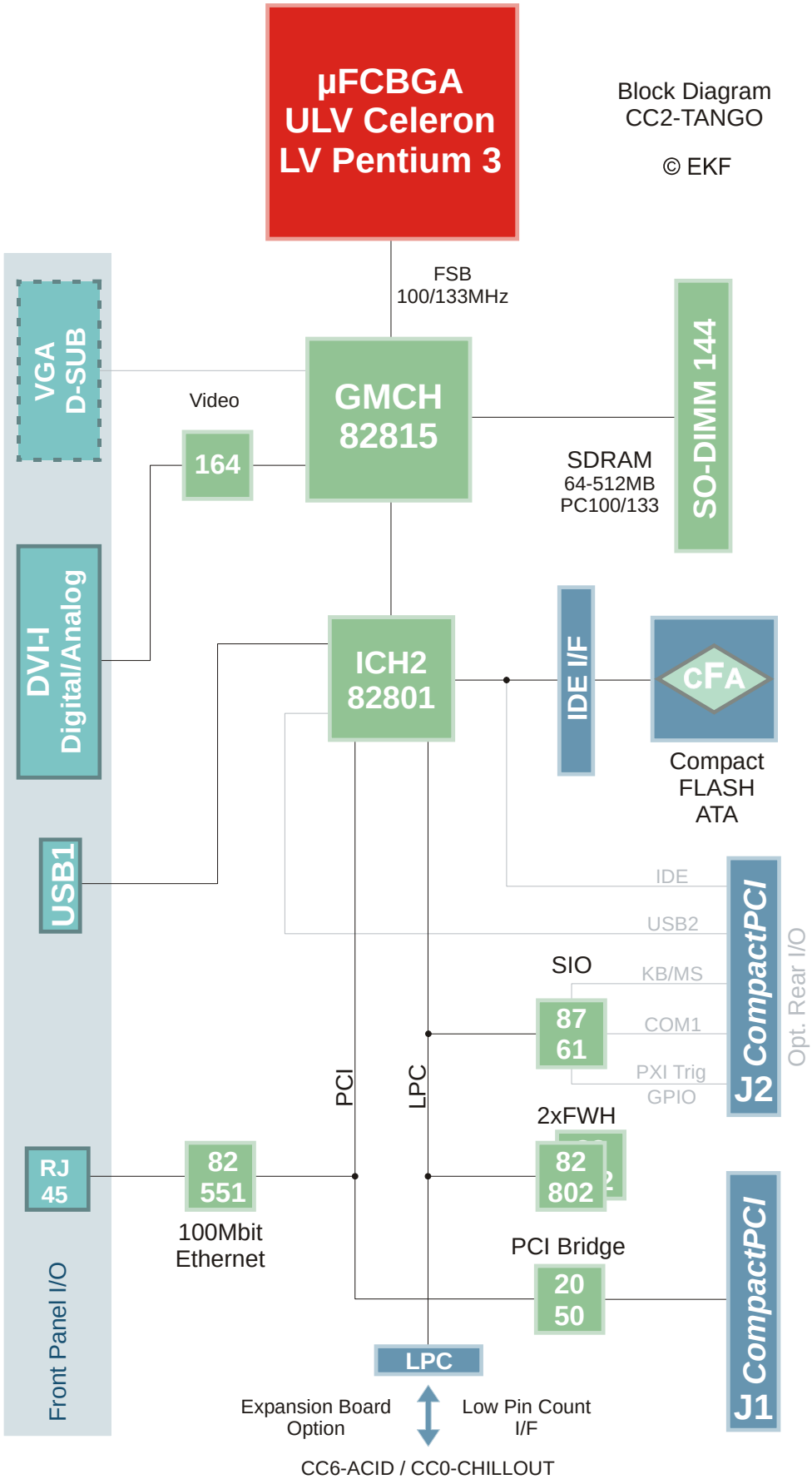
Block Diagram CC2-TANGO



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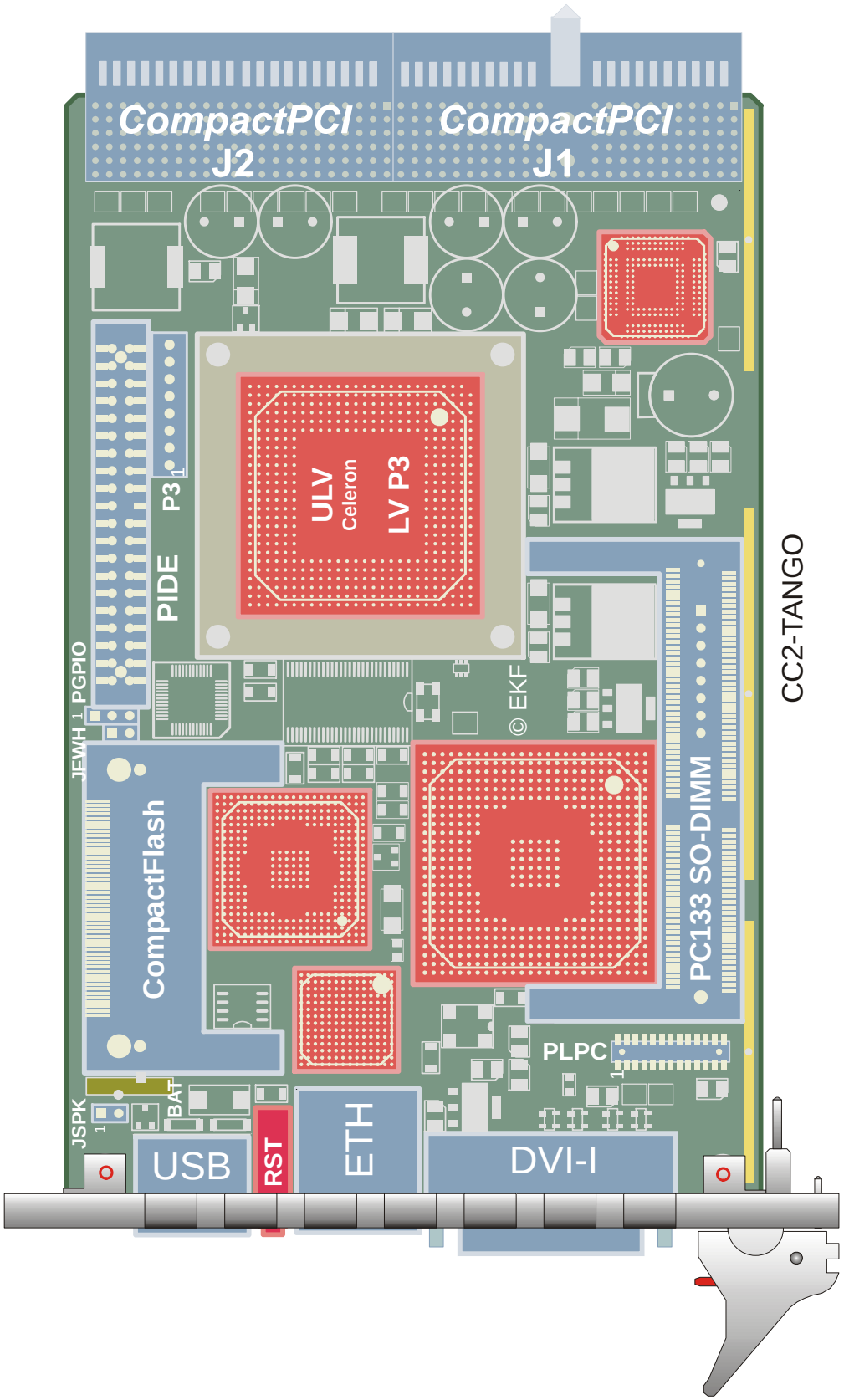
Top View Component Assembly CC2-TANGO



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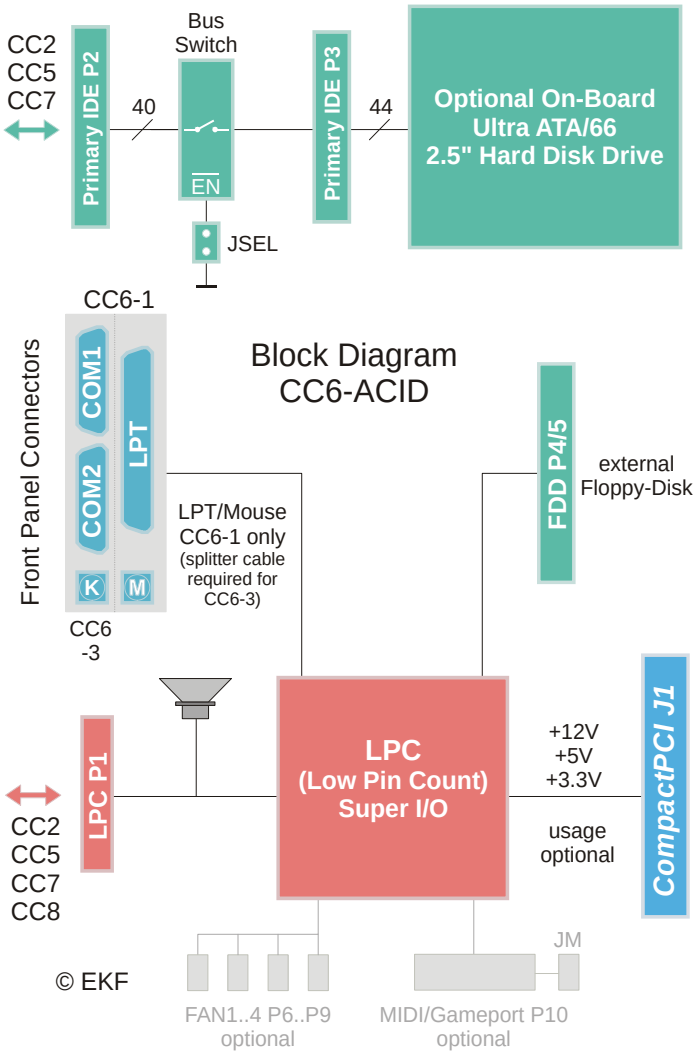
Expansion Modules CC6-ACID & CC0-CHILLOUT

Available as a companion board to the CC2-TANGO, the CC6-ACID is provided with several legacy I/O ports. This module can be mounted either to the bottom side or on top of the CC2-TANGO and communicates across the LPC (Low Pin Count) interface.

The CC6-ACID will be required only if the classical interfaces, e.g. serial and parallel port remain in use in a given application.

As an option, the CC6-ACID can be delivered with an on-board 2.5" hard disk drive, resulting in a very compact system. The connectors COM1/2, LPT, mouse and keyboard are situated at the front panel (4HP and 8HP versions available), while an external floppy disk drive can be attached via the on-board pin header.

The CC0-CHILLOUT is similar to the CC6-ACID, but destined for use together with a rear I/O transition module (CCZ-RIO).



CC6-ACID Block Diagram

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CC6-ACID (4HP)

CC6-ACID (8HP)

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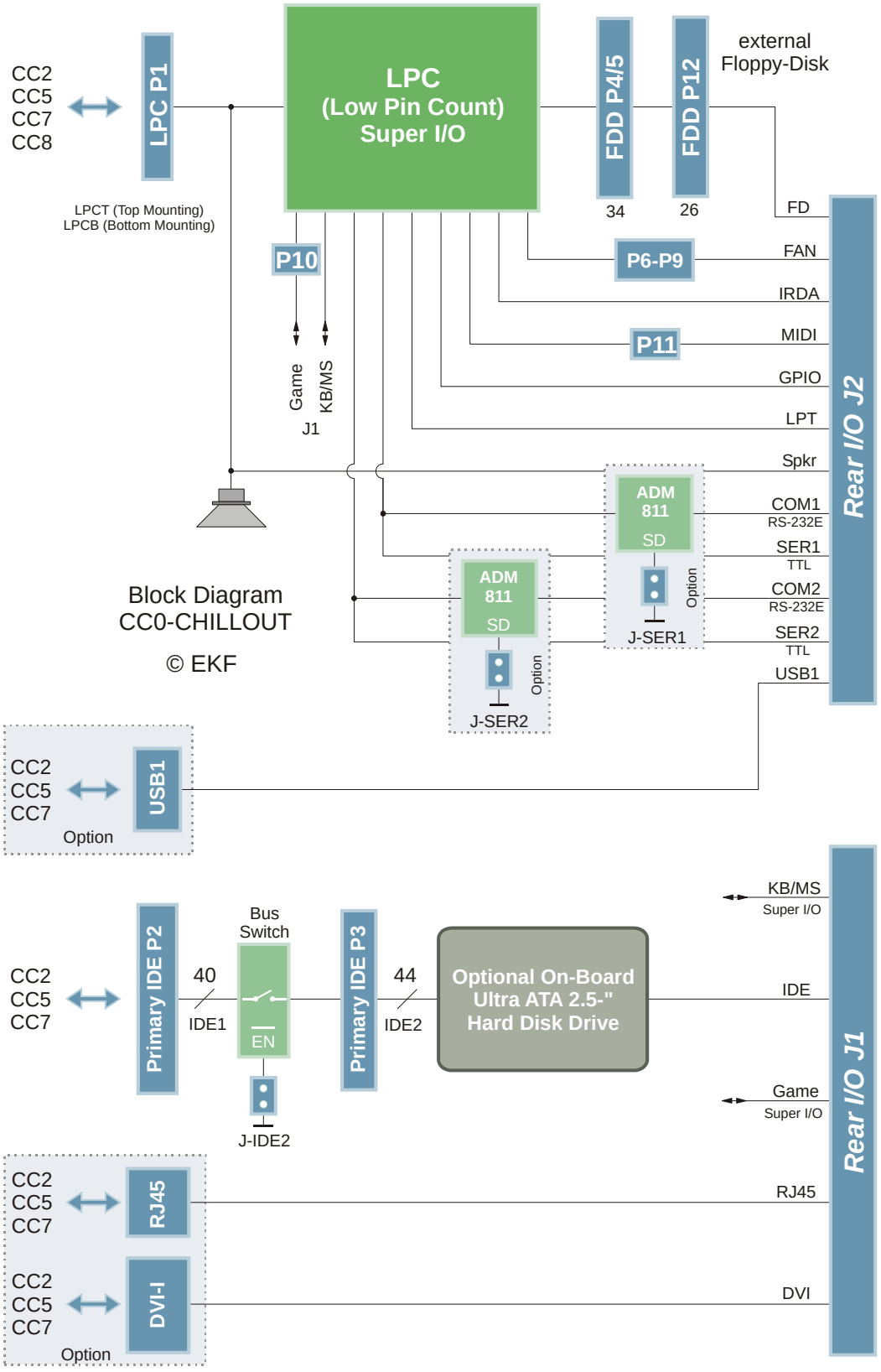

CC0-CHILLOUT Block Diagram

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Computer Cartridge CCF-CONCERT

In addition to the CC6-ACID with its on-board hard disk drive, the CC2-TANGO can be combined with a slim-line floppy disk drive. This CompactPCI computer is named CCF-CONCERT.

Housed in a 3U cassette, the entire computer requires only 12HP mounting space, while surpassing the whole functionality of a PC.

CCF-CONCERT

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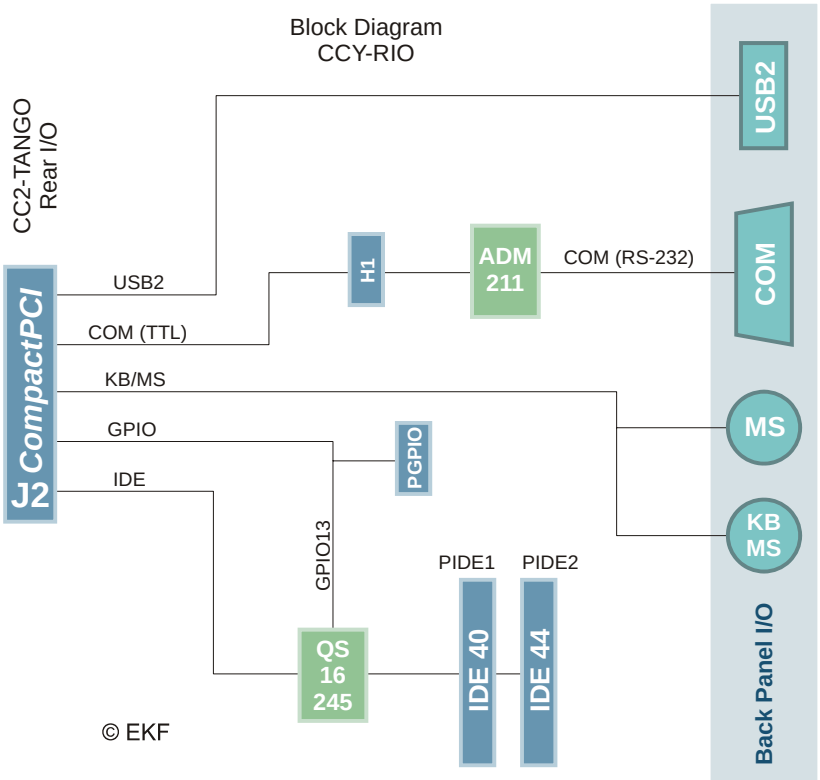
Rear I/O Transition Module CCY-RIO

Available as an option, the CC2-TANGO can be delivered for rear I/O utilization. Several I/O ports can be routed across the J2 connector. Rear I/O requires that a suitable J2 backplane is present in your CompactPCI system. By default, the CC2-TANGO is equipped with line terminating resistors for a common 64-bit CPCI J2 backplane.

The CCY-RIO rear I/O transition module provides a 4HP back panel with connectors for PS/2 style keyboard and mouse, a serial RS-232E COM port, and an USB receptacle.

In addition, optional on-board headers are stuffed on the CCY-RIO for attachment of IDE/ATA devices (hard disks, DVD ROM drives).



Block Diagram CCY-RIO

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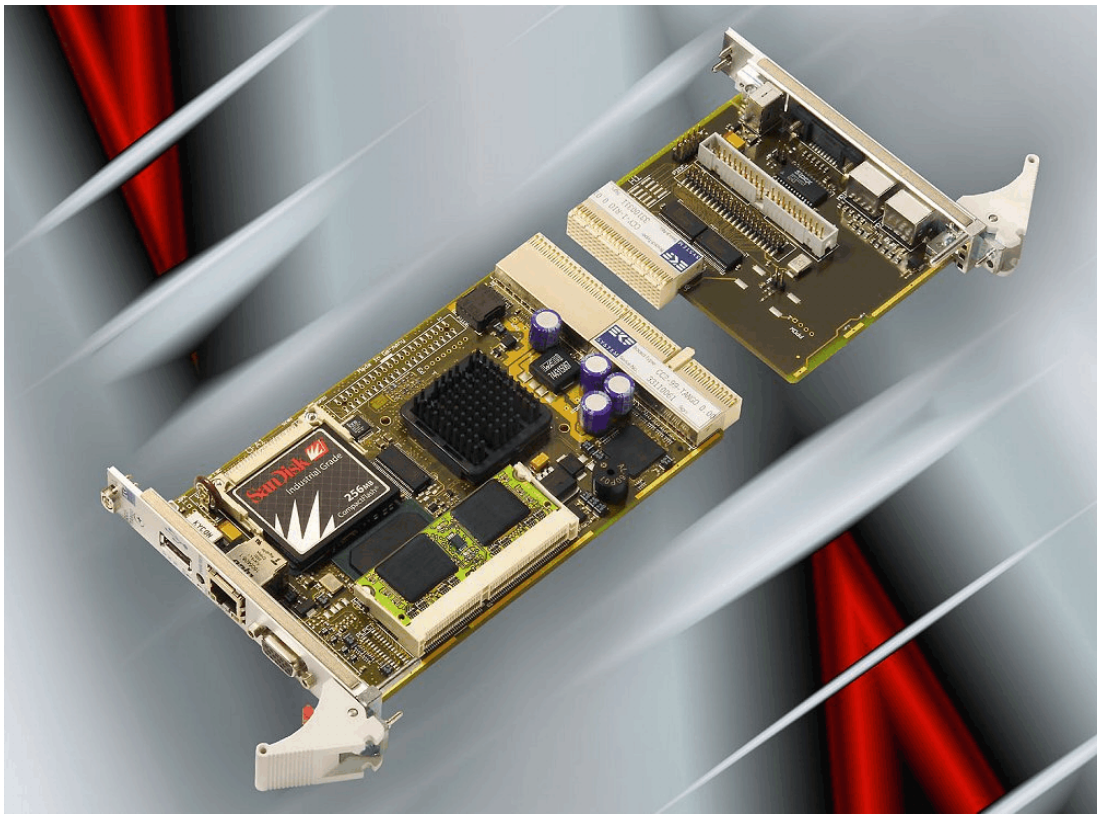
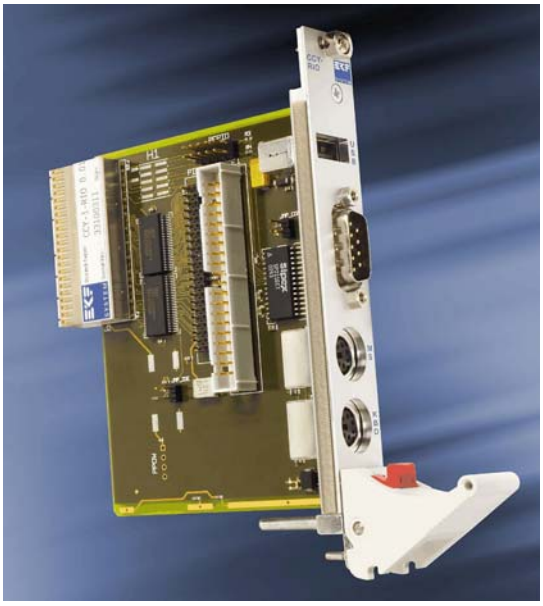


CC2-TANGO & CCY-RIO



CCY-RIO

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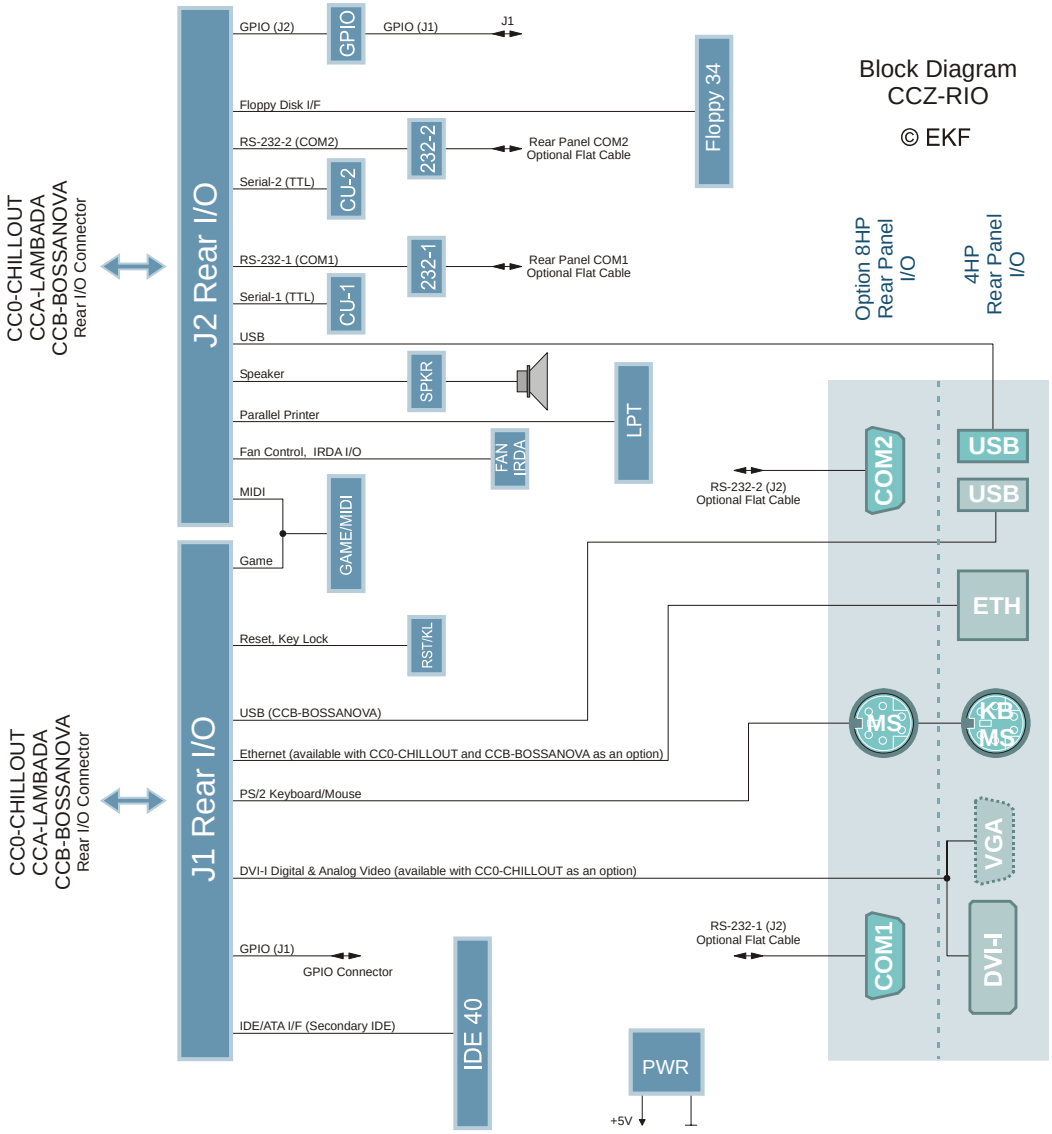
Rear I/O Transition Module CCZ-RIO

Available as an option, the CC2-TANGO can be combined with the CC0-CHILLOUT companion board, which has been designed mainly for rear I/O systems. Therefore the CCZ-RIO is required in addition for passing signals across a single slot rear I/O backplane to the rear panel.

The CCZ-RIO rear I/O transition module provides a 4HP back panel (8HP option) with connectors for PS/2 style keyboard and mouse, an USB receptacle and optionally Ethernet and video connectors. In addition, optional on-board headers are stuffed on the CCZ-RIO for attachment of various devices.



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Strapping Headers

ISPCON	In System Programmable GAL (PLD programming), not stuffed
PGPIO	Local GPIO signals derived from the on-board SIO, option
JSPKR	Speaker connector, option
JFWH	Firmware hub selection, option
JRTC	CMOS and RTC reset

Connectors & Sockets

CFA1	CompactFlash ATA socket (secondary IDE interface)
J1/J2	*CompactPCI* Bus, PXI, Rear I/O
PLPCT PLPCB	Low Pin Count expansion interface connector (Super-I/O), available either from top (T) or bottom (B) of the board
PIDE	Ultra ATA/100 connector (primary IDE interface)
PITP	CPU Debug Port, not stuffed
SODIMM1	144-pin memory module SDRAM PC133
P3	Power connector for stand-alone operation, not stuffed

Front Panel Elements

Ethernet	100Base-TX/10Base-T, RJ-45 receptacle with integrated indicator LEDs
Graphics	DVI-I integrated (digital & analog) receptacle, suitable for DVI digital flat panel displays and/or analog monitors
USB	Universal Serial Bus 1.1 self powered root hub, type A receptacle
Reset	Push-button switch with integrated indicator LED (power good)
IDE	LED indicating IDE activity
GPIO	Special purpose LED

Microprocessor

The CC2-TANGO supports the 0.13µ Ultra Low-Voltage (ULV) Celeron® and Low-Voltage (LV) Pentium®-III processors as listed below. The processors are housed in a Micro FC-BGA package for direct soldering to the PCB, i.e. the CPU chip cannot be removed or changed by the user.

Do not confuse the processor host bus frequency (FSB front side bus or PSB processor side bus) with the memory speed or the PCI clock, which are independent from each other. The ULV Celeron processors support 100MHz FSB clock, while the LV Pentium III processors are designed for 133MHz FSB clock. The internal CPU speed is achieved by multiplying the host bus frequency by a fixed value.

The CC2-TANGO is powered across the CompactPCI connectors J1 (3.3V, 5V). The processor core voltage is generated by a switched voltage regulator, sourced from the 5V plane. The ULV Celeron processors signal their required core voltage by 5 dedicated pins according to the IMVPII specification, which can be directly used to control the settings of the voltage regulator. The required core voltage for the LV Pentium III processors however, complying to the VRM8.5 specification, must be adjusted by a couple of resistors on the CC2-TANGO. The core voltage settings actually in use can also be read back by several GPIO lines of the ICH2.

ULV Celeron® 0.13µ Processors Supported							
Processor	Speed	Host Bus	L2 Cache	CPU ID	Package	Stepping	sSpec
Celeron	400MHz	100MHz	256KB	06b1h	µFCBGA	FBA1	SL6SE
Celeron	650MHz	100MHz	256KB	06b4h	µFCBGA	FBB1	SL6B8

Low Voltage Pentium® III 0.13µ Processors Supported							
Processor	Speed	Host Bus	L2 Cache	CPU ID	Package	Stepping	sSpec
Pentium III	800MHz	133MHz	512KB	06b4h	µFCBGA	tB1	SL6HC
Pentium III	933MHz	133MHz	512KB	06b4h	µFCBGA	tB1	SL69K

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Thermal Considerations

In order to avoid malfunctioning of the CC2-TANGO, take care of appropriate cooling of the processor and system, e.g. by a cooling fan suitable to the maximum power consumption of the CPU chip actually in use. Please note, that the processors temperature is steadily measured by a special controller (MAX1617), attached to the onboard SMBus® (System Management Bus). The processor core (die) temperature is signalled by the forward voltage of a CPU integrated diode. A second diode internal to the MAX1617 allows for acquisition of the boards surface temperature. The programmable over-temperature alarm allows to trigger the SMBus alert line in order to avoid overheating. A suitable software to display both, the die temperature, as well as the board temperature, is MBM (Motherboard Monitor), which can be downloaded from the web. After installation, both temperatures can be observed permanently from the Windows taskbar.

By default, the CC2-TANGO is equipped with a passive heatsink. Its height takes into account the 4HP limitation in mounting space of a CPCI board. In addition, a forced vertical airflow through the system enclosure (e.g. bottom mount fan unit) is strongly recommended (>15m^3/h or 200LFM around the CPU slot). As an exception, the CC2-1-TANGO (ULV Celeron 400MHz) can be operated with natural convection only. Be sure to thoroughly discuss your actual cooling needs with EKF. Generally, the faster the CPU speed the higher its power consumption. For higher ambient temperatures, consider increasing the forced airflow to 400 or 600LFM. A non-standard heatsink also could improve (lower) the thermal resistance between the die and the environment (requires more than 4HP board pitch, depending from the heatsink in use).

The maximum power consumption and operating temperature of a particular processor can be derived from the tables below. Fortunately, the power consumption is by far lower when executing typical Windows or Linux tasks. The heat dissipation increases especially when rendering software is executed, e.g. the Acrobat Distiller. EKF tests the CC2-TANGO by running a proprietary Intel tool for generating the maximum stress to the processor.

ULV Celeron® 0.13□ Processors Power Consumption and Die Temperature				
Processor	Speed	Typ. Power	Max. Power	Die Temperature
Celeron	400MHz	3.40W	4.23W	0-100°C
Celeron	650MHz	7.00W	8.30W	0-100°C

LV Pentium® III 0.13□ Processors Power Consumption and Die Temperature				
Processor	Speed	Typ. Power	Max. Power	Die Temperature
Pentium III	800MHz		11.2W	0-100°
Pentium III	933MHz		12.2W	0-100°

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The CC2-TANGO can be equipped with either a heatsink according to the option 2 described in the Intel Thermal Design Guide, which must be fixed by four mounting fasteners, or a snap-on heat spreader, which is fixed by a clip directly to the BGA.

The forced airflow thermal resistance of the snap-on heatsink is 4.6K/W @ 200lfm, 2.7K/W @ 400lfm and 2.0K/W @ 600lfm. With no forced airflow (natural convection) the heat sink thermal resistance is ~13.8K/W. With 100°C as maximum specified die temperature, the worst case ambient temperatures for the CC2-TANGO can be calculated a follows:

Maximum Permissible Ambient Temperature					
Processor	Max. Power	0 LFM	200 LFM	400 LFM	600 LFM
ULV Celeron 400MHz	4.23W	41.5°C	*80.5°C*	*88.5°C*	*91.5°C*
ULV Celeron 650MHz	8.3W	-	61.5°C	*77.5°C*	*83.0°C*
LV Pentium III 800MHz	11.2W	-	48.0°C	69.5°C	*77.5°C*
LV Pentium III 933MHz	12.2W	-	43.5°C	67.0°C	*75.0°C*

Temperatures marked italic/grey:
Nominal values only, the board should not be operated permanently beyond 70°C

As it can be seen, natural convection cooling is an option for the CC2-1-TANGO only, which is equipped with the ULV Celeron 400MHz processor. Forced airflow cooling between 200lfm (ULV Celeron) and 400lfm (LV Pentium III) is recommended for typical operation of the board.

A special method to reduce power consumption and therefore increasing the maximum ambient temperature, is to force the processor into the 'Throttle Mode'. This is achieved by actuating the 'Stop Clock' input of the CPU, and can be activated through the BIOS settings. A Throttle Mode of 50% e.g. means a duty cycle of 50% on the stop clock input. However, while saving a certain amount in power consumption, the data throughput of the processor is also reduced.

Main Memory

The CC2-TANGO is equipped with a socket for installing a single 144-pin SO-DIMM module. Minimum memory size is 32MB; maximum memory size is 512MB. Due to the video requirements of the i815 chipset, minimum memory for the Windows NT 4.0 and Windows 2000 operating system is 64MB (some of the system memory is dedicated to the graphics controller). The supported on-board memory is entirely chacheable. The memory module is a unbuffered SD-RAM, PC133 style. The contents of the SPD Eeprom are displayed on system start by the BIOS. The memory clock is 133MHz maximum, due to limitations of the 815GMCH (Graphics and Memory Controller Hub).

The GMCH is sometimes also referenced as 'Northbridge'. No special drivers are needed for the memory controller portion of the GMCH - configuration is done by the BIOS and the operating system.

LAN Subsystem

The CC2-TANGO is equipped with the 82551ER 100Mbps Ethernet controllerFeatures include:

- PCI bus mastering 32-bit, 33MHz
- 100Base-TX (Fast Ethernet, half- or full-duplex) and 10Base-T (Classic Ethernet) capability using a single RJ-45 connector
- IEEE 802.3 Auto-Negotiation for the fastest available connection
- Jumperless configuration (complete software-configurable)

Two display LEDs integrated into the RJ-45 connector signal the LAN connection speed and the LAN link and activity status.

The NIC (Networking Interface Controller) resides on the local PCI bus. Its MAC address (unique hardware number) is stored in an EEPROM. The Intel Ethernet software and drivers for the 82551ER are available from Intel's World Wide Web site for download.

Enhanced IDE Interface

The EIDE interface handles the exchange of information between the processor and peripheral devices like hard disks, ATA CompactFlash cards and CD-ROM drives. The interface supports:

- Up to three ATA devices (2 IDE, 1 CompactFlash)
- PIO Mode 3/4, Ultra ATA/33, Ultra ATA/66, Ultra ATA/100
- Support for LS-120 drives

The primary IDE interface is routed to a standard 40-position header (2.54mm pitch), allowing master and slave device attached to one common flat ribbon cable (use special 80-pin cabling assembly for Ultra ATA/66 and Ultra ATA/100 operation).

The presence of an 80-pin cable at the primary IDE interface could be checked out by reading the state of the GPI1 of the Firmware Hub (FWH). The ATA standard defines the signal PDIAG-/CBLID- for identifying the cable. This line is routed to GPI1 of the FWH. A logical 1 signals a 40-pin, a logical 0 a 80-pin cable. See the ATA/ATAPI-6 specification (section 6.7 "Host determination of cable type by detecting CBLID-") for details.

As an alternate, the primary IDE port is optionally also available for rear I/O across the J2/P2 CompactPCI connector.

The secondary IDE interface is routed to the CompactFlash Card Adapter socket. Use this connector to attach a CompactFlash ATA style silicon disk, whenever a hard disk is not suitable for your system, or as an additional mass storage device.

A display LED, situated in the front panel near the reset push-button, signals disk activity status of the primary IDE devices and also the CompactFlash slot. This LED is also software programmable. See the section "Programmable LED" how to do this.

The IDE controller is integrated into the i801 ICH2 (I/O Controller Hub 2). The ICH2 is sometimes also referenced as 'Southbridge'. Ultra ATA IDE drivers can be downloaded from the Intel website.

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Graphics Subsystem

The graphics subsystem is part of the Intel 82815 Graphics/Memory Controller Hub (GMCH), supporting the following features:

- 3-D Hyper Pipelined architecture
- Full 2-D hardware acceleration
- Motion video acceleration
- 3-D graphics visual and texturing enhancements
- Integrated 24-bit 230MHz RAMDAC
- DDC2B compliant
- Hardware motion compensation for software MPEG2 decode
- Integrated graphics memory controller

The CC2-TANGO is provided with the DVI-I graphics connector. This is both a digital and analog interface. Recent digital input flat-panel displays are widely available with this connector style (e.g. the NEC Mitsubishi Ambix series). For classic monitors, adapters or adapter cables can be used for converting from DVI-I to the 15-pin HD D-SUB connector.

A special display transmitter chip is used for serializing/deserializing the differential DVI signals. The SiI 164 (Silicon Image) transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface. The SiI 164 transmitter has a highly flexible interface with 12-bit (½ pixel/clock) or 24-bit (1 pixel/clock) input for true color (16.7 million) support. It can be foreseen, that DVI will overcome the legacy analog and proprietary digital interfaces in the near future.

The GMCH supports several video resolutions and refresh rates. A partial list is contained in the table below. Please note, that flat-panel displays should be operated with their maximum resolution at 60Hz refresh rate.

i815 GMCH Video Modes and Clock Rates (Partial List)					
Resolution/ Refresh Rate	60Hz	70Hz	72Hz	75Hz	85Hz
640x480	25.175MHz	28MHz	31.5MHz	31.5MHz	36MHz
800x600	40MHz	45MHz	50MHz	49.5MHz	56.25MHz
1024x768	*65MHz*	75MHz	-	78.75MHz	94.5MHz
1152x864	80MHz	96MHz	99MHz	108MHz	121MHz
1280x1024	*108MHz*	128.89MHz	132MHz	135MHz	157.5MHz
1600x1200	162MHz	189MHz	195MHz	202.5MHz	229.5MHz

Video modes marked italic/blue: Suitable for popular flat-panel displays

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As an option, the CC2-TANGO can be equipped with an ordinary HD D-Sub 15-lead connector (VGA style). This connector is suitable for analog signals only, so the PanelLink transmitter is not stuffed with this option. Nevertheless also flat-panel displays can be attached to the D-Sub connector with only minor impact on the image quality.

Independent from the video connector actually in use, DVI or VGA, the VESA DDC 2B standard is supported. This is a two-wire serial bus (clock, data), which is controlled by the GMCH and allows to read out important parameters, e.g. the maximum allowable resolution, from the attached monitor. In addition, DDC Power (+5V) is delivered to either connector. Resettable fuses are stuffed to protect the board from an external short-circuit condition (0.75A for DVI, 2 x 0.75A for VGA).

Graphics drivers for the i815 GMC can be downloaded from the Intel website.

Real-Time Clock

The CC2-TANGO has a time-of-day clock and 100-year calendar, integrated into the ICH2. A battery on the board keeps the clock current when the computer is turned off. The CC2 uses a Vanadium-Pentoxide-Lithium rechargeable battery, giving an autonomy of more than 80 days when fully loaded after 24 hours. The cell is free of memory effects and withstands deep discharging. Under normal conditions, replacement should be superfluous during lifetime of the board. The RTC registers can be manually reset by the jumper JRTC.

Universal Serial Bus (USB)

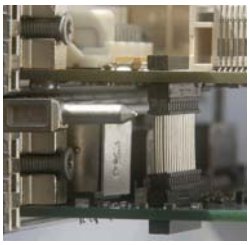
The CC2-TANGO is provided with two USB 1.1 ports. One USB I/F is routed to a front panel connector, while the other is optionally available for rear I/O across the J2/P2 CompactPCI connector. When using both ports, you can connect a maximum of two USB peripheral devices directly to the CC2 without an external hub. To attach more devices, get an external hub connected to one of the CC2 USB ports. Both, the front panel USB connector and the rear I/O USB interface can source up to 0.5A/5V to external devices, over-current protected by an electronic switch. Both USB controllers are integrated into the i801 ICH2.

LPC Super- I/O Interface

In a modern system, legacy ports as PS/2 keyboard/mouse, COM1/2 and LPT have been replaced by USB and Ethernet connectivity. The 1.4MB floppy disk drive has been swapped against LS-120 or CD-RW drives, attached to the IDE connector, or USB memory sticks. Hence, the CC2-TANGO is virtually provided with all necessary I/O ports. However, for compatibility purposes the CC2 is additionally equipped with a simple Super-I/O chip, for optional rear I/O of PS/2 keyboard/mouse and COM1 (TTL level only) across the J2/P2 CPCI connector. The Super-I/O controller resides on the local LPC bus (LPC = Low Pin Count interface standard), which is a serialized ISA bus replacement.

As an alternative, EKF offers the CC6-ACID, an expansion module to the CC2-TANGO, featuring all classic Super-I/O functionality. The CC6-ACID is a 3U Eurocard, with an either 8HP (double) or 4HP (single) width front panel. Access to the connectors COM1/2, LPT, mouse, keyboard is given directly from the front panel. On board connectors are provided for FDD, MIDI/Gameport, and cooling fans. Optionally, the CC6 is available with an onboard 2.5" hard disk drive. The CC6-ACID connects to the CC2-TANGO across the connector LPCT or LPCB. The CC6-ACID can be attached either to the top of the CC2-TANGO or to the bottom (bottom attachment restricted to the 4HP version of the CC6-ACID).

The photo above (left) shows the bottom attachment of the CC6-ACID. The boards are fixed together by the LPC connector and the IDE connector, and in addition by a bracket which bolts together both front panels. The right image shows the top attachment of the CC6-ACID.



The photo above (left) shows the CC2-TANGO and CC6-ACID connected by the LPC interface. The right image shows the front panel fixing bracket.

Together, the CC2-TANGO and the CC6-ACID form an ultra-compact, complete desktop functionality, industrial grade computer system.

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Watchdog/Reset

The CC2-TANGO is provided with two MAX6705 supervisor circuits, which monitor the supply voltages 3.3V and 5V, and generate a power-on reset signal. The manual push-button reset is also passed through the MAX6705s for appropriate pulse conditioning.

The reset manual push-button is situated at the front panel. The button is indent mounted behind the front and requires a tool, e.g. pen to be pressed, preventing from being inadvertently activated. The push button reset signal is routed across a PLD (programmable logic device) and could be passivated on customers request.

The healthy state of the CC2-TANGO is signalled by the LED PWR integrated into the reset push-button. As soon as this LED begins to shine all power voltages are well and the reset signal has been deasserted.

Another feature is the watchdog function, which can be be programmed by software. The behaviour of the MAX6705 watchdog is partially defined by the PLD, which controls whether the watchdog is activated. The related software (e.g. BIOS, application program) must trigger the watchdog by toggling the GPO21 signal of the ICH2.

The watchdog is in a passive state after a system reset. There is no need to trigger it at boot time. Once the GPO21 of the ICH2 has sent a pulse, the watchdog is activated. If the duration between two trigger pulses exceeds a period of 1000ms, the watchdog times out and a system reset will be generated.

The watchdog remains in the active state until the next system reset. There is no way to disable it once it was started.

Firmware Hub (Flash BIOS)

The BIOS is stored in one or two 82802 8Mbit Firmware Hubs (there are second sources in use with deviant part numbers). Each firmware hub contains a nonvolatile memory core based on flash technology, allowing the BIOS to be upgraded. If a second FWH is stuffed, the Jumper JFWH allows to select between the devices (JFWH removed: boot from FWH1, JFWH set: boot from FWH2).

The FWH can be reprogrammed (if suitable) by a DOS based tool. This program and the latest CC2-TANGO BIOS are available from the EKF website. Read carefully the enclosed instructions. If the programming procedure fails e.g caused by a power interruption, the CC2-TANGO may no more be operable. If a second FWH is installed, you may recover from this situation by selecting the remaining FWH. Otherwise you would have to send in the board, because the BIOS is directly soldered to the PCB and cannot be changed by a typical user.

IDE (Hard Disk Activity) LED

The CC2-TANGO offers a software programmable LED, marked as IDE (placed near the reset push-button). After system reset, this LED defaults to signal the IDE activity. By the first setting of the GPO22 of the ICH2 82801 this LED changes its function and is then controlled only by the level of the GPO22 pin. Setting this output to 1 will switch on the LED.

The LED IDE remains in the programmable state until the next system reset.

GP (General Purpose) LED

A second programmable LED can be also observed from the front panel. The status of the GP LED is controlled by the GPO23 output of the ICH2. As of current, the GP LED is not dedicated to any particular hardware or firmware function (this may change in the future). It is therefore user programmable.

Hot Swap Detection

The CompactPCI specification added the signal ENUM# to the PCI bus to allow the system hot swapping. This signal is routed to the GPI6 of the ICH2 82801 on the CC2-TANGO. A System Management Interrupt (SMI) can be requested if ENUM# changes by insertion or removal of a board.

Note that the CC2-TANGO itself isn't a hot swap device, because it makes no sense to remove the system controller from a CompactPCI system. However, it is capable to recognize the hot swap of peripheral boards and to start software that is doing any necessary system reconfiguration.

Power Supply Status (DEG#, FAL#)

Power supply failures may be detected before the system crashes down by monitoring the signals DEG# or FAL#. These active low lines are additions of the CompactPCI specification and may be driven by the power supply.

DEG# signals the degrading of the supply voltages, FAL# there possible failure.

On the CC2-TANGO FAL# is routed to the GPI0 and DEG# to the GPI1 of the ICH2 82801.

PXI Trigger Signals

As an option, the CC2-TANGO supports four of the eight trigger signals of the PXI standard, as defined by National Instruments. The trigger signals are provided by the local SIO (Super-I/O) chip. GPIO20/21 are routed to TRIG0/1, and GPIO26/27 are used to control TRIG6/7. These signals can also be used as GPIO lines in a non-PXI environment.

Local GPIO Option

In addition to the GPIO / PXI-Trigger lines optionally available on J2, the optional pin-header PGPIO provides another two GPIO lines available for user specific application. The 5V TTL signals sio_gpio16/17 are controlled by the on-board SIO IT8761E, with an internal 50k PU resistor and capable of sinking 24mA each.

Rear I/O Options

Optionally, the CC2-TANGO can be used for rear I/O with respect to the following functions:

- Primary IDE
- USB Port 2
- Keyboard, Mouse
- COM1 (TTL Level)
- GPIOs

If attachment of IDE devices across the rear I/O path is chosen, the CC2-TANGO on-board IDE connector must be removed or at least not be used, in order to avoid a T-connection. The rear I/O USB port is independent from the front panel USB connector by using its own controller integrated into the ICH2, thus doubling the overall USB bandwidth available. Keyboard and mouse as well as the serial interface and the GPIOs require the on-board SIO to be stuffed. The COM1 port does not include the physical transceiver (TTL level only). The GPIOs are used as trigger signals in a PXI system, but can also be utilized for general applications in a non-PXI environment. Each of the above functions can be activated individually (by appropriate stuffing/removing of resistor networks).

Utilization of the CCY-RIO rear I/O transition module is bound to several preconditions, which must be completely satisfied.

- The CC2 CPU card by default is suitable for a 64-bit CompactPCI backplane. However, the J2/P2 pin assignments of a 64-bit CPCI backplane differ substantially from a CompactPCI rear I/O backplane. Hence usage of the rear I/O features is available only as stuffing options on the CC2 CPU board, which have to be ordered explicitly. Pull-up resistor networks on the CPCI address/data lines AD33-AD63 and associated control signals must be removed, and pass-through resistor networks for the required rear I/O signals have to be filled on the CC2. Neither can these modifications be made afterwards on a CC2 64-bit J2 CPU board by the user, nor by EKF, due to the technical effort needed and costs incurred.

- The system in use must be equipped with a P2 CompactPCI rear I/O backplane. If the system is provided with a P2 CompactPCI 64-bit backplane instead, several of the CC2 rear I/O signals will collide with the 64-bit address/data lines on the backplane, with unpredictable results regarding the rear I/O signal integrity.

Please note, that EKF is not only a manufacturer of boards, but also has many years of experience as a system integrator. Please contact sales@ekf.de for a quote on the complete system, tailored to your individual needs.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for rapair.

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Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

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Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system

- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

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EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

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Installing or Replacing the Memory Module

Note: If you decide to replace the memory, observe the precautions in 'Before You Begin'

By default, the CC2-TANGO comes fully equipped and tested with a 256MB/512MB SD-RAM memory module. So normally there should be no need to install a memory module.

The CC2-TANGO requires a PC-133 (133MHz) SDRAM SO-DIMM module independent from the processor front side bus (100MHz ULV Celeron, 133MHz LV Pentium III). It is highly recommended that Serial Presence Detect (SPD) SO-DIMMs be used, since this allows the chipset to accurately configure the memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

A replacement memory module must match the 144-pin SO-DIMM form factor (known from Notebook PCs), 3.3V, 133MHz unbuffered, non-ECC style. Be sure to buy no module with a height >1.250 inch (31.75mm). Suitable modules are available up to 512MB. The 815GMCH supports modules of up to a maximum of 13 address lines (A0...A12). Memory modules organized by more than13 address lines are not suitable.

Replacement of the Battery

When your system is turned off, a battery maintains the current time-of-day clock and the values in CMOS RAM current. The battery is rechargeable und should last during the lifetime of the CC2-TANGO. For replacement, the old battery must be desoldered, and the new one soldered. Observe the cell polarization. We suggest that you send back the board to EKF for battery replacement.

Warning

Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type. Do not expose a battery to fire.

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Technical Reference

Local PCI Devices

The following table shows the on-board PCI devices and their location within the PCI configuration space. These devices consist of the Ethernet controller, the PCI-To-PCI Bridge and several devices within the i815 chip set.

Bus Number	Device Number	Function Number	Vendor ID	Device ID	Description
0	0x00	0	0x8086	0x7120	Host Bridge
0	0x01	0	0x8086	0x7121	VGA Display
0	0x1E	0	0x8086	0x2418	PCI-To-PCI Bridge
0	0x1F	0	0x8086	0x2410	ISA Bridge
0	0x1F	1	0x8086	0x2411	IDE Controller
0	0x1F	2	0x8086	0x2412	USB Controller
0	0x1F	3	0x8086	0x2413	SMB Controller
1	0x04	0	0x8086	0x1209	Ethernet Controller
1	0x06	0	0x104C	0xAC28	PCI-To-PCI Bridge (CPCI)

Local SMB Devices

The CC2-TANGO contains a few devices that are reachable via the System Management Bus (SMB). These are the clock generation chip, the SPD EEPROM on the SO-DIMM memory module and a CPU temperature controlling device in particular. Other devices could be connected to the SMB via the *CompactPCI* signals IPMB SCL (J1 B17) and IPMB SDA (J1 C17).

Address	Description
0x30	CPU Temperature Sensor MAX 1617
0xA0	SPD of SO-DIMM
0xD2	Main Clock Generation ICS 9250-16
0xA4	Board EEPROM 24C04

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GPIO Usage

GPIO Usage ICH2

CC2-TANGO GPIO Usage ICH2			
Function	CC2	Features	Origin/Destination
p2_fal#	GPI 0 ICH2	I (5V tol.)	CPCI Power Mgmt.
p2_deg#	GPI 1 ICH2	I (5V tol.)	CPCI Power Mgmt.
pirqe#	GPI 2 ICH2	I	LAN NC1
pirqf#	GPI 3 ICH2	(5V tol.)	CPCI INTC#
pirqg#	GPI 4 ICH2	(5V tol.)	CPCI INTD#
pirqh#	GPI 5 ICH2	I	ICH2 USB2
p1_enum#	GPI 6 ICH2	I (5V tol.)	CPCI
-	GPI 7 ICH2	I (5V tol.)	-
Vid4	GPI 8 ICH2	I	Core Voltage Regulator (read only)
-	intruder#	I	-
smbalrt#	GPI 11 ICH2	I	SMB
lsmi# (LPC)	GPI 12 ICH2	I	SIO (LPC)
lpme# (LPC)	GPI 13 ICH2	I	SIO (LPC)
	GPO 16 ICH2	O (int. PU)	
p2_trg7	GPO 17 ICH2	O (int. PU)	
-	GPO 18 ICH2	O	-
-	GPO 19 ICH2	O	-
-	GPO 20 ICH2	O	-
wdi#	GPO 21 ICH2	O	ispGAL
gpo22 (ispGAL)	GPO 22 ICH2	OD	ispGAL
gpo23 (ispGAL)	GPO 23 ICH2	O	ispGAL
Vid0	GPIO 24 ICH2	I/O	Core Voltage Regulator (r/w)
Vid1	GPIO 25 ICH2	I/O	Core Voltage Regulator (r/w)
Vid2	GPIO 27 ICH2	I/O	Core Voltage Regulator (r/w)
Vid3/4	GPIO 28 ICH2	I/O	Core Voltage Regulator (r/w)

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GPIO Usage FWH

CC2-TANGO GPIO Usage FWH			
Function	**FWH**	**Features**	**Origin/Destination**
FWH1/FWH2 Identity	GPI 0 FWH	I (3.3V)	GND = FWH1 3.3V = FWH2
p66detect (IDE)	GPI 1 FWH	I (3.3V)	IDE I/F
wdogrst	GPI 2 FWH	I (3.3V)	ispGAL
MSB Board Revision	GPI 3 FWH	I (3.3V)	GPI3 GPI4 Rev. 0 0 0 0 1 1 1 0 2 1 1 3+
LSB Board Revision	GPI 4 FWH	I (3.3V)	

GPIO Usage SIO

CC2-TANGO GPIO Usage SIO			
Function	**SIO**	**Features**	**Origin/Destination**
p2_brsva15	GPIO 13 SIO	I/O (5V int. PU 8mA)	Rear I/O Module Detection J2/P2
-	GPIO 14 SIO	I/O (5V int. PU 8mA)	
-	GPIO 15 SIO	I/O (5V int. PU 8mA)	
sio_gpio16	GPIO 16 SIO	I/O (5V int. PU 24mA)	PGPIO
sio_gpio17	GPIO 17 SIO	I/O (5V int. PU 24mA)	PGPIO
p2_brsvb16	GPIO 20 SIO	I/O (5V int. PU 8mA)	PXI TRIG0 J2/P2
p2_brsva16	GPIO 21SIO	I/O (5V int. PU 8mA)	PXI TRIG1 J2/P2
-	GPIO 22 SIO	I/O (5V int. PU 24mA)	
-	GPIO 23 SIO	I/O (5V int. PU 24mA)	
-	GPIO 24 SIO	I/O (5V int. PU 24mA)	
-	GPIO 25 SIO	I/O (5V int. PU 24mA)	
p2_brsve18	GPIO 26 SIO	I/O (5V int. PU 24mA)	PXI TRIG6 J2/P2
p2_brsve16	GPIO 27 SIO	I/O (5V int. PU 24mA)	PXI TRIG7 J2/P2

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GPIO Usage PCI Bridge

CC2-TANGO GPIO Usage PCI-PCI Bridge			
Function	2050	Features	Origin/Destination
p2_sysen#	GPIO 0	I/O (5V tol.)	CPCI
enintp	GPIO 1	I/O (5V tol.)	ispGAL
enints	GPIO 2	I/O (5V tol.)	ispGAL
enserirq	GPIO 3 / HSSWITCH#	I/O (5V tol.)	CPCI, ispGAL

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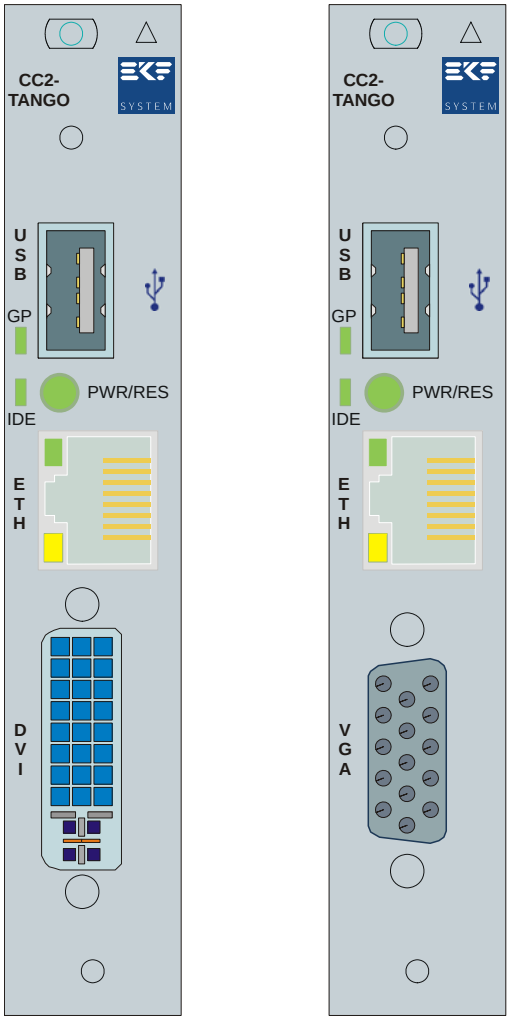
Connectors

Caution

Some of the internal connectors provide operating voltage (e.g. 5V and 12V) to devices inside the system chassis, such as fans and internal peripherals. Not all of these connectors are overcurrent protected. Do not use these internal connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Front Panel Connectors



CC2-TANGO Front Panel Elements

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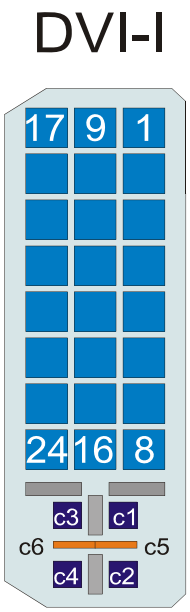
Video Monitor Connector DVI-I

DVI-I					
17	tx0-	9	tx1-	1	tx2-
18	tx0+	10	tx1+	2	tx2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	ddcpow	6	ddccl
23	txc+	15	GND	7	ddcda
24	txc-	16	dvihp	8	vsync

c3	blue	c1	red	
c6	GND	c5	GND	
c4	hsync	c2	green	



For attachment of an ordinary analog RGB monitor to the DVI receptacle, there are both adapters and also adapter cables available from DVI-I to the HD-SUB15 connector. Attachment of digital monitors (flat panel displays) should be done by means of a DVI to DVI cable (single link style cable is sufficient).

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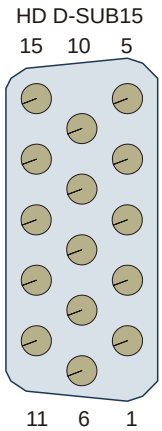
Video Monitor Connector HD-DSUB (Option)

As an option, the CC2-TANGO can be equipped with a legacy VGA connector (High-Density D-Sub 15-position female connector). The VGA connector replaces the DVI receptacle, and the digital video interface therefore is not available with this option.

VGA1	
1	red
2	green
3	blue
4	nc
5	GND
6	GND
7	GND
8	GND
9	+5V (PolySwitch 1.5A) DDC Power
10	GND
11	nc
12	DDC Data
13	Hsync
14	Vsync
15	DDC Clock



VGA
Connector Option

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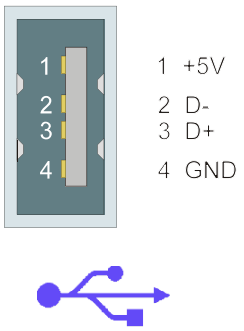
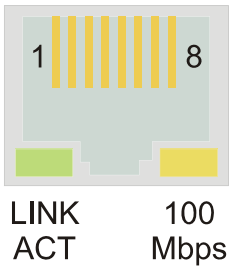
USB Connector

1	+5V (Electronic Switch 0.5A)
2	USB Data NEG
3	USB Data POS
4	GND



Ethernet Connector

RJ45	
1	TX+
2	TX-
3	RX+
4	
5	
6	RX-
7	
8	



The yellow LED signals 100Mbit/s when lit, and 10Mbit/s when off. The green LED indicates LINK established when continuously on, and data transfer (activity) when blinking. If the green LED is off, no LINK is established.

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Internal Connectors

LPC Low Pin Count Header

PLPCT/PLPCB			
GND	1	2	pciclk
GND	3	4	lad0
GND	5	6	lad1
GND	7	8	lad2
GND	9	10	lad3
GND	11	12	lframe#
GND	13	14	ldrq#
serirq	15	16	lpme#
lsmi#	17	18	pcirst#
5V	19	20	3.3V
rcin#	21	22	a20gate
12V	23	24	3.3V
sio_clk14	25	26	speaker

The LPC header is available twice, on both sides of the board, top and bottom, in order to provide attachment of the CC6-ACID either to the left or to the right side of the CC2-TANGO. Warning: Neither the +12V pin, nor the +5V pin, nor the +3.3V pin are protected against a short circuit situation! This connector therefore should be used exclusively for attachment of the CC6-ACID board.

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ATA/IDE Header

PIDE			
reset#	1	2	GND
pd07	3	4	pd08
pd06	5	6	pd09
pd05	7	8	pd10
pd04	9	10	pd11
pd03	11	12	pd12
pd02	13	14	pd13
pd01	15	16	pd14
pd00	17	18	pd15
GND	19	20	KEY
pdmarq	21	22	GND
piow#	23	24	GND
pior#	25	26	GND
piordy	27	28	GND
pdmack#	29	30	GND
intrq (IRQ 14)	31	32	
pda1	33	34	p66detect
pda0	35	36	pda2
pcs0#	37	38	pcs1#
pideact#	39	40	GND

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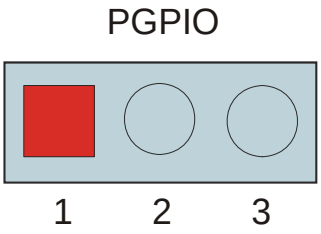
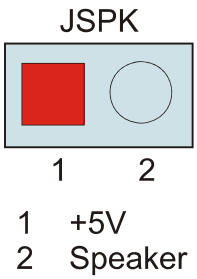
Local GPIO Header (Option)



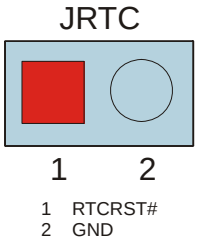
Both GPIO signals are 5V TTL with internal 50k PU resistors, 24mA sink capability, controlled by the on-board SIO IT8761E.

Speaker Header (Option)



Warning: The +5V pin is protected against a short circuit situation by a 0.1A PolySwitch. The JSPK connector should be used exclusively for direct attachment of a dynamic speaker device. When connecting to the input of a sound card, most likely a short-circuit situation will occur between the +5V pin of the JSPK connector and the GND pin of the audio-card input, which could cause permanent damage to the CC2-TANGO and the audio board, despite the PolySwitch resettable fuse. A workaround to this would be to place a 1k resistor across pin 1 and pin 2 of the JSPK connector, and strapping a single wire cable from JSPK pin 2 to the audio input.

RTC/CMOS Reset Jumper (Option)



If stuffed, the jumper JRTC can be used to clear the CMOS contents and to reset the RTC registers. Remove jumper for normal operation.

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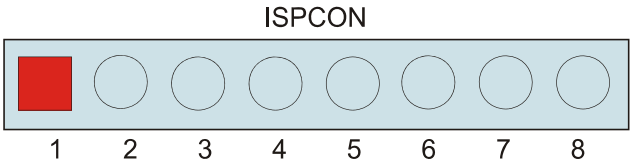
PLD Programming Header



1 +5V
2 serial data out
3 serial data in
4 ispGAL enable
5 NC
6 mode
7 GND
8 serial clock

Note: The ISPCON is not normally stuffed. Its footprint is situated at the bottom side of the board.

Processor Debug Header

JITP			
itpres#	2	1	GND
dbreset#	4	3	GND
tck	6	5	GND
tms	8	7	tdi
itppon	10	9	tdo
	12	11	trst#
GND	14	13	
GND	16	15	itpreq#
GND	18	17	itprdy#
GND	20	19	
GND	22	21	
GND	24	23	
GND	26	25	
GND	28	27	
GND	30	29	

Note: The Debug Header is not normally stuffed. Its footprint is situated at the bottom side of the board.

CompactPCI J1

#J1	A	B	C	D	E
25	5V	*REQ64#*	ENUM#	3.3V	5V
24	AD1	5V	VI/O	AD0	*ACK64#*
23	3.3V	AD4	AD3	5V	AD2
22	AD7	GND	3.3V	AD6	AD5
21	3.3V	AD9	AD8	M66EN (GND)	C/BE0#
20	AD12	GND	VI/O	AD11	AD10
19	3.3V	AD15	AD14	GND	AD13
18	SERR#	GND	3.3V	PAR	C/BE1#
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
15	3.3V	FRAME#	IRDY#	GND	TRDY#
14					
13					
12					
11	AD18	AD17	AD16	GND	C/BE2#
10	AD21	GND	3.3V	AD20	AD19
9	C/BE3#	IDSEL	AD23	GND	AD22
8	AD26	GND	VI/O	AD25	AD24
7	AD30	AD29	AD28	GND	AD27
6	REQ#	GND	3.3V	CLK	AD31
5	*BRSVP1A5*	*BRSVP1B5*	RST#	GND	GNT#
4	IPMB PWR	GND	VI/O	INTP	INTS
3	INTA#	INTB#	INTC#	5V	INTD#
2	*TCK*	5V	*TMS*	*TDO*	*TDI*
1	5V	-12V	*TRST#*	+12V	5V

pin positions printed italic/coloured brown: not connected
pin positions printed italic/coloured blue: not connected
pin positions printed italic/coloured gray: pull up 1k to Vio

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CompactPCI J2

#J2	A	B	C	D	E
22	*GA4*	*GA3*	*GA2*	*GA1*	*GA0*
21	CLK6	GND	*RSV* KB_DAT	*RSV* KB/MS_POW	*RSV* MS_DAT
20	CLK5	GND	*RSV* KB_CLK	GND	*RSV* MS_CLK
19	GND	GND	*RSV* COM1_TXD	*RSV* COM1_RXD	*RSV* COM1_RTS#
18	*BRSVP2A18*	*BRSVP2B18*	*BRSVP2C18*	GND	*BRSVP2E18* PXI_TRIG6
17	*BRSVP2A17*	GND	PRST#	REQ6#	GNT6#
16	*BRSVP2A16* PXI_TRIG1	*BRSVP2B16* PXI_TRIG0	DEG#	GND	*BRSVP2E16* PXI_TRIG7
15	*BRSVP2A15* MOD_DET#	GND	FAL#	REQ5#	GNT5#
14	*AD35* IDE_RST#	*AD34* IDE_D7	*AD33* IDE_D8	GND	*AD32* IDE_D6
13	*AD38* IDE_D9	GND	V(I/O)	*AD37* IDE_D5	*AD36* IDE_D10
12	*AD42* IDE_D4	*AD41* IDE_D11	*AD40* IDE_D3	GND	*AD39* IDE_D12
11	*AD45* IDE_D2	GND	V(I/O)	*AD44* IDE_D13	*AD43* IDE_D1
10	*AD49* IDE_D14	*AD48* IDE_D0	*AD47* IDE_D15	GND	*AD46* IDE_DRQ
9	*AD52* IDE_IOW#	GND	V(I/O)	*AD51* IDE_IOR#	*AD50* IDE_IORDY
8	*AD56* IDE_DACK#	*AD55* IDE_INT	*AD54* IDE_A1	GND	*AD53* IDE_66MHz
7	*AD59* IDE_A0	GND	V(I/O)	*AD58* IDE_A2	*AD57* IDE_CS1#
6	*AD63* IDE_CS3#	*AD62* IDE_ACT#	*AD61* COM1_CTS#	GND	*AD60* COM1_DSR#
5	*C/BE5#* COM1_DTR#	GND (64EN#)	V(I/O)	*C/BE4#* USB2_POW	*PAR64* USB2_D+
4	V(I/O)	*BRSVP2B4* +5V/0.75A	*C/BE7#* COM1_DCD#	GND	*C/BE6#* *USB2_D-*
3	CLK4	GND	GNT3#	REQ4#	GNT4#
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#
1	CLK1	GND	REQ1#	GNT1#	REQ2#

pin positions printed italic/coloured gray: 1k to Vio
pin positions printed italic/coloured brown: not connected
pin positions printed blue: rear I/O options
pin positions printed green: PXI Trigger options

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Power Connector P3 (Option)

P3 (Option)	
1	+5V
2	+5V
3	GND
4	GND
5	GND
6	GND
7	+3.3V
8	+3.3V

This connector is optional for stand-alone operation of the CC2-TANGO (not normally stuffed). It is a 2.50mm pitch eight position pin header, AMP Tyco EI series part no. 171825-8. Refer to the Tyco website for suitable matching components. If P3 is in use for power supply, J1/J2 are not needed for stand-alone operation.

Literature

Theme	Document Title	Origin
CompactPCI	*CompactPCI* Specification, PICMG 2.0 R3.0, Oct. 1, 1999	PICMG (http://www.picmg.org)
USB	Universal Serial Bus Specification	http://www.usb.org/developers/docs/
CompactFlash	CF+and CompactFlash Specification Revision 2.0	CompactFlash Association www.compactflash.org

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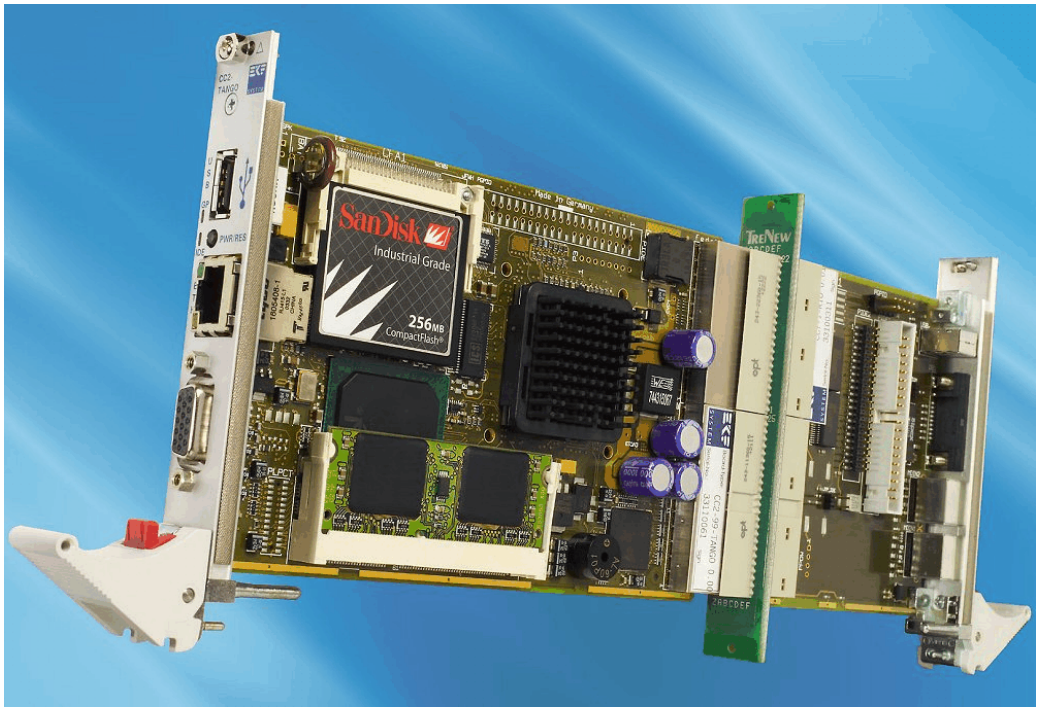

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